DAQ

660*x* Register-Level Programmer Manual

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Register Maps

About This Manual

The *660x Register-Level Programmer Manual* describes the programmable features of the 660*x* devices and is necessary for programmers using platforms not supported by NI-DAQ.

This manual contains the following information necessary to perform register-level programming for the 660*x* devices:

- Address and function 660*x* device registers for reading and writing data, and for configuring the input lines and the general-purpose counter/timers (GPCTs)
- Overview of several common GPCT operations
- Guidelines for configuring GPCTs

Note Use the change notification feature *only* if you are familiar with writing, installing, and uninstalling interrupt service routines.

National Instruments recommends programming the 660*x* device using NI-DAQ with application development environment software, such as LabVIEW, LabWindows/CVI, or Measurement Studio. Application software provides easier programming with the same flexibility as register-level programming and much faster development time.

Using the Manual Set

The *660x Register-Level Programmer Manual* is one piece of the documentation set for your data acquisition system. For information about a specific 660*x* device, refer to the user manual for that device. The user manual provides installation procedures, connection requirements, programming options, specifications, and guidelines for operating the 660*x* devices.

Consult the accessory installation guides or manuals for information about accessory products. The terminal block and cable assembly installation guides or accessory board user manuals explain how to connect system parts.

Conventions

This manual uses the following conventions:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIG+0.<3..0>.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes sections of code, programming examples, and syntax examples. This font is also used for the proper names of programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *6601/6602 User Manual*
- *Note to Users: About Your 6608 Device*
- *PXI Specification,* Revision 1.0
- *PICMG CompactPCI 2.0 R2.1*

1

About the 660*x* Devices

This chapter provides a summary of the National Instruments 660*x* devices and includes a brief overview of the MITE and NI-TIO components.

The National Instruments 660*x* devices are timing and digital I/O boards for use with the PCI bus in PC-compatible computers and PXI or CompactPCI chassis.

The 6601 device features four 32-bit counter channels and eight lines of individually configurable, TTL/CMOS-compatible digital I/O. The 6602 and 6608 devices have the same capabilities as the 6601 device, but feature eight 32-bit counter channels and an 80 MHz clock. The 6608 device features an oven-controlled crystal oscillator (OCXO) for greater timing accuracy.

Refer to the *6601/6602 User Manual* or the *Note to Users: About Your 6608 Device* for more information about device functionality, installation, connections, and safety guidelines.

Caution Using the 660*x* devices in a way inconsistent with the *6601/6602 User Manual* and the *Note to Users: About Your 6608 Device* can cause injury or equipment damage. National Instruments is *not* liable for damage or injury resulting from incorrect use.

Caution Incorrectly programming the 660*x* devices can cause permanent damage to the devices. For example, some I/O pins can be driven from several outputs. Two sources driving the same I/O pin could burn out the I/O pin and destroy one of the ASICs. Because 6602 and 6608 devices have two NI-TIO ASICs, they are particularly subject to this kind of damage. If using both ASICs, configure the second NI-TIO to use the I/O pins for the second NI-TIO. Doing so prevents both NI-TIOs from connecting to the same I/O pins.

Structural Overview

The following functional groups make up the 660*x* circuitry:

- MITE PCI interface ASIC
- NI-TIO (0) general-purpose counter/timer (GPCT) ASIC
- NI-TIO (1) general-purpose counter/timer ASIC, available on the 6602 and 6608 devices only

Figure 1-1 illustrates the data flow of the 660*x* devices.

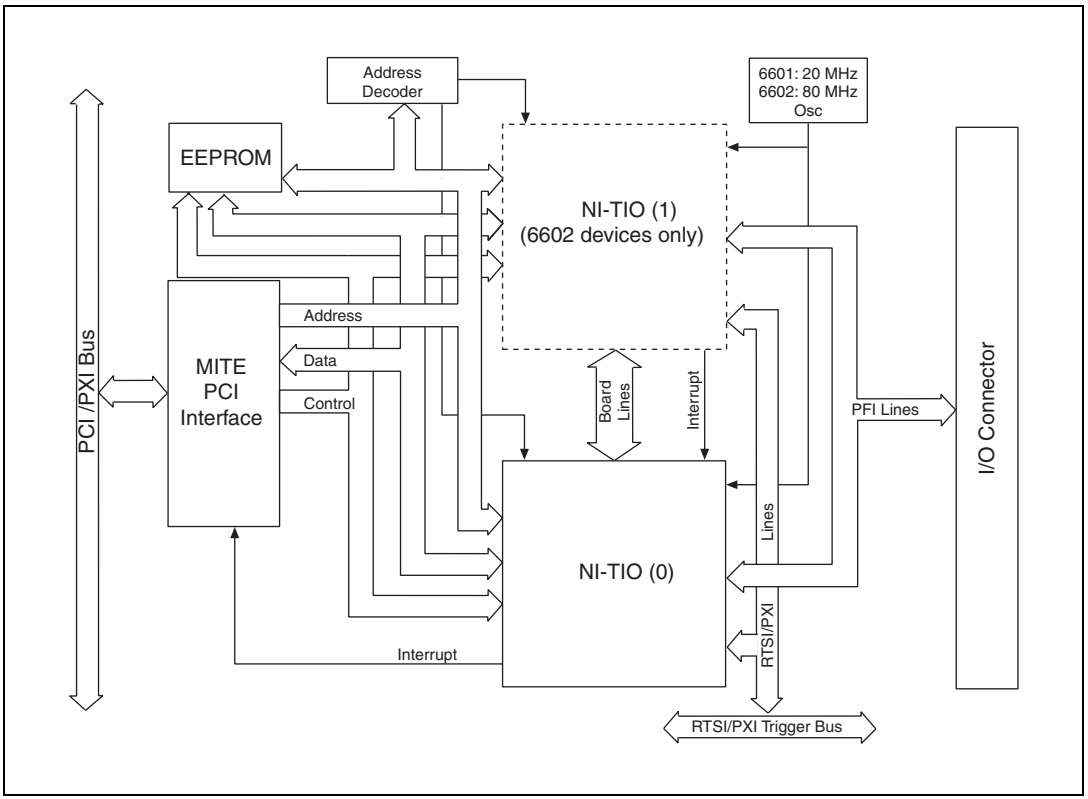

Figure 1-1. 660*x* Device Data Flow

MITE PCI Interface ASIC

The MITE PCI Interface ASIC is the interface for register accesses, interrupts, and DMA. The MITE enables communication between the 660*x* device and the PCI or PXI bus. Once initialized, the MITE enables communication with other 660*x* device components.

NI-TIO General-Purpose Counter/Timer ASIC

Each National Instruments NI-TIO GPCT ASIC contains four general-purpose counters that are independent of one another. Each counter has a source, two gates, an output, and multiple load registers. The 6601 device has one NI-TIO—NI-TIO (0)—while the 6602 and 6608 devices have two NI-TIOs—NI-TIO (0) and NI-TIO (1).

Caution To avoid double-driving the counter outputs on the 6602 and 6608 devices, use Counter Swap in the Clock Config Register to configure the second NI-TIO to use counters 4 through 7. If configured incorrectly, both NI-TIOs will use the I/O connectors for counters 0 through 3, which could permanently damage the device.

NI-TIO GPCTs

Each NI-TIO consists of four independent 32-bit up/down counters. These counters are identical, except for the internal routing of the counter outputs and inputs. Each counter has associated load and save registers and a control structure for implementing some common counting and timing I/O functions. The timing functions include period measurement, pulse-width measurement, event counting, single-pulse generation, and pulse-train generation with programmable frequency and duty cycle.

Note Most functions can operate using only one general-purpose counter.

Measurement functions have two operational modes: single mode and buffered mode. Single mode functions obtain only one measurement, while buffered mode functions obtain a series of consecutive, gap-free measurements.

You can select the GPCT input signals from the external timing I/O pins on the 660*x* devices. Available input options depend on the type of GPCT input. Output generation and timing measurement are the two primary GPCT modes.

Features

The NI-TIO has the following features:

- Four independent 32-bit binary up/down counters
- Count-up/count-down control through hardware or software
- Programmable counter source and gate selection from 19 signal sources
- Programmable input and output signal polarities

- Single pulse or continuous pulse generation output
- Inter-event (relative) timestamping
- Two sets of save registers to save the counter value through an external control signal or through software command
- Current count value readings that do not affect circuit operation
- Interrupts based on terminal count (TC)—rising edge, falling edge, or any edge
- Quadrature encoder position measurements

Note The 660*x* devices do *not* support BCD counting and time-of-day counting.

Simplified Model

The GPCT contains four identical 32-bit binary up/down counters. Figure 1-2 shows a simplified model of the GPCT.

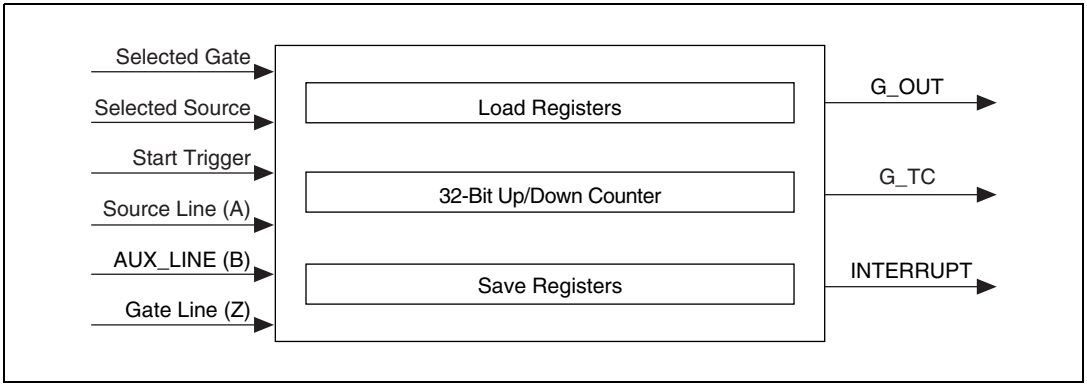

Figure 1-2. General-Purpose Counter/Timer Simplified Model

Each GPCT counter has a source input (Selected Source), a gate input (Selected Gate), and a second gate input (AUX_LINE) that doubles as an up/down control input. When the counter is enabled, rising edges on the Selected Source input cause the counter to increment or decrement. The Selected Gate input acts as a general-purpose control signal and can operate as a counter trigger signal, a counter enable, a save signal, a reload signal, an interrupt, an output control signal, a load register select signal, or a counter disarm. The AUX_LINE can determine whether the counter counts up or down.

The counter outputs are the signals labeled G_OUT and INTERRUPT. G_OUT is a counter TC-related signal that can toggle on every counter TC or output the counter TC signal directly. INTERRUPT is an interrupt signal routed to the MITE. The load registers reload the counter with new count values, and the save registers save the counter contents until the software can read them.

Pulse Generation

In pulse generation mode, the counter decrements until reaching terminal count, the output of the counter changes, and a load register reloads the counter. The source may be a known frequency, in which case both the duty cycle and the output frequency are known. The source may also be an input that needs to be divided by an integer. The operation may be single-shot, repetitive, or triggered from the gate signal.

The NI-TIO has four available load registers—Load A and Load B in two X and Y bank cells. With this flexibility, you can generate any duty cycle and reprogram the load registers to change the properties on the fly. The output is typically programmed to alternate on each terminal count, but it can be programmed to toggle on the terminal count signal to create the smallest pulse or highest frequency output.

Figure 1-3 illustrates the pulse generation data flow.

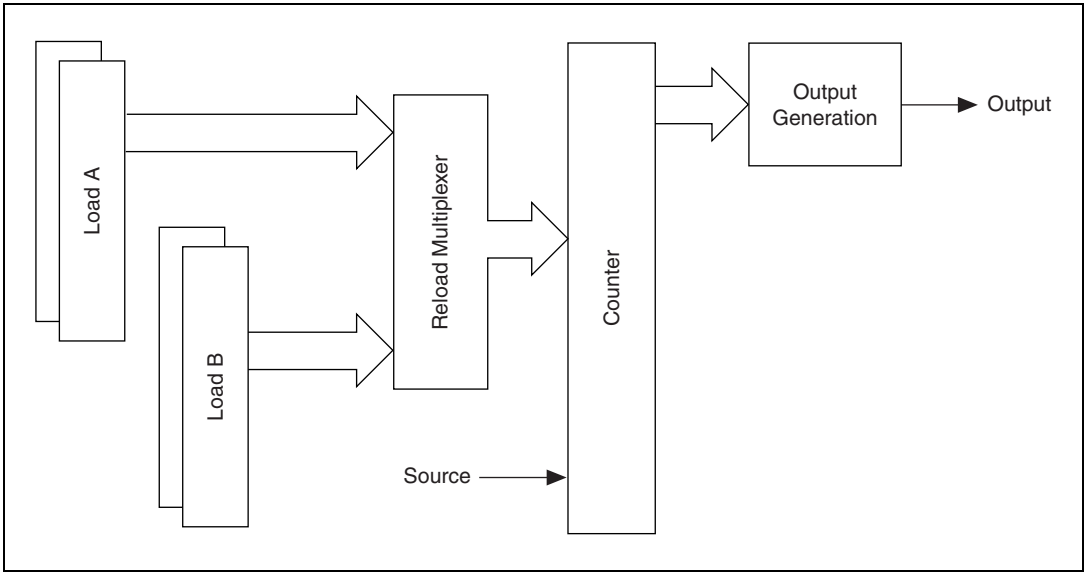

Figure 1-3. Pulse Generation Data Flow

Measurement

In measurement modes, the counter measures the source or the gate properties. Source edges increment or decrement the counter, and the gate signal stops and starts the counter. During buffered acquisitions, the gate signal also latches the counter state for either a software or DMA reading of the measurement. For measurements such as period, semi-period, or pulse width, the counter uses a known timebase (usually the fastest internal timebase) for clocking, and the Gate signal starts and stops the counter while latching the measurement. With event counting and frequency measurements, an unknown signal applied to the source and the gate is of a fixed time to create a window of measurement.

Figure 1-4 illustrates the measurement data flow.

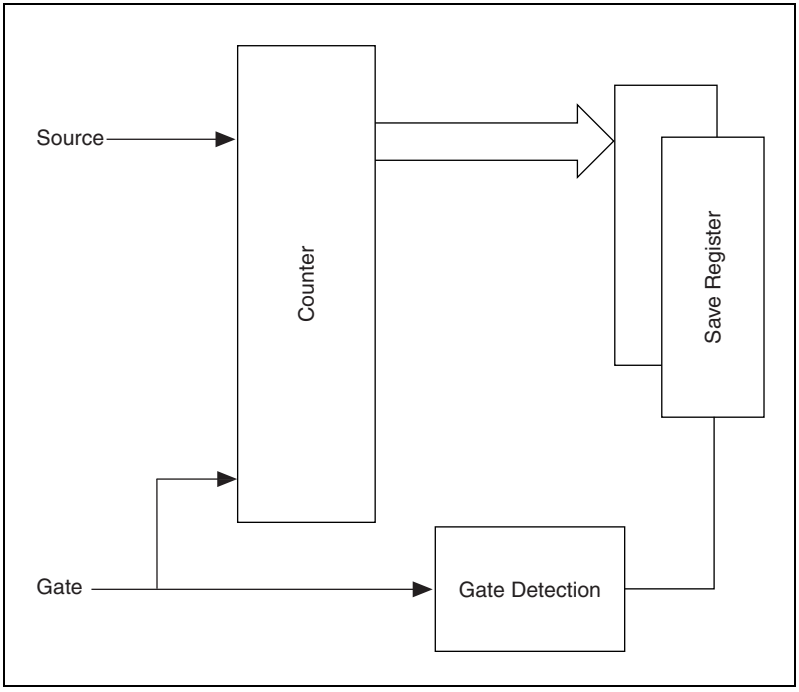

Figure 1-4. Measurement Data Flow

Oscillator

The signal from the oscillator is the internal timebase for the 660*x* devices. The 6601 device uses 20 MHz oscillators, and the 6602 and 6608 devices use an 80 MHz oscillator.

EEPROM

The EEPROM stores PCI plug-and-play configuration information. The MITE reads this memory during system boot.

RTSI

The NI-TIO ASICs can access the RTSI bus to share triggers or to clock signals between DAQ devices. The RTSI on 6602 and 6608 devices can share triggers between the two NI-TIOs.

Note Only one NI-TIO or 660*x* device should drive a RTSI line at a time. Double-driving a RTSI line can damage the 660*x* device.

Other Features

The NI-TIO includes several other features for specific measurement or generation cases, including an interface to quadrature encoders for position and velocity measurement of rotating devices. Additionally, the NI-TIO second gate allows edge separation measurements.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature of the *PXI Specification,* revision 1.0. Using a PXI-compatible plug-in device in a standard CompactPCI chassis enables you to use basic plug-in device functions, but PXI-specific functions are not available. For example, the RTSI bus on PXI-660*x* devices is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification enables vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses or between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The PXI-6602 and PXI-6608 devices work in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R2.1* specification.

The J2 connector of the CompactPCI bus implements the PXI-specific features. The PXI device is compatible with any CompactPCI chassis whose sub-bus does not drive these lines.

Caution Driving these lines with the sub-bus may cause damage to the 660*x* device.

Even if the sub-bus is capable of driving these lines, the PXI device is still compatible with the CompactPCI chassis if the pins on the sub-bus are disabled by default. Refer to Table 1-1 for a list of the J2 pins the PXI-6602 device uses.

Table 1-1. Pins Used by PXI-660*x* Devices

PXI-6602/6608 Signal	PXI Pin Name	PXI J2 Pin Number
RTSI Trigger (0..5)	PXI Trigger (0..5)	B16, A16, A17, A18, B18, C18
RTSI Trigger (6)	PXI Star	D17
RTSI Clock	PXI Trigger (7)	E16
Reserved	LBR (7, 8, 10, 11, 12)	A3, C3, E3, A2, B2

2

General-Purpose Counter/Timers

This chapter contains a functional overview of the GPCT, as well as register-level programming examples that illustrate the functions described in this chapter.

Functional Overview

You can use the 660*x* device in the counter-based applications outlined in Table 2-1. For more detailed descriptions of each application, refer to Chapter 3, *Device Overview*, of the *6601/6602 User Manual*.

Table 2-1. Counter-Based Applications

Application Class	Application
Simple Counting	Simple event counting Gated-event counting
Time Measurement	Single-period measurement Single pulse-width measurement Two-signal edge-separation measurement
Simple Pulse and Pulse-Train Generation	Single pulse generation Single-triggered pulse generation Retriggerable single pulse generation Continuous pulse-train generation
Buffered Counting and Time Measurement	Buffered event counting (continuous) Buffered period measurement (continuous) Buffered semiperiod measurement (continuous) Buffered pulse-width measurement (continuous) Buffered two-signal edge-separation measurement (continuous)
Position Measurement	Quadrature encoders
Miscellaneous Functions	Digital I/O

Reading Counter Values

This section explains how to read the values for disarmed and armed counters, and how to take buffered readings from counters.

Disarmed Counters

Read the SW Save register to determine the counter value on a disarmed counter. Use this method for single-period and single pulse measurements.

Armed Counters

Values for armed counters can change during the register read. If disarming the counter is impractical, as with simple event counting or position measurement, read the SW Save register twice. If both reads are the same, their value indicates the counter value. If the two reads are different, the counter value changed during one of the register reads. In this case, read the SW Save register a third time. The third read is the correct counter value.

Buffered Readings

During a buffered measurement, the counter must save a value and continue counting. Setting the G*i* DMA Enable bit in the G*i* DMA Config register tells the counter to save the counter contents in either the HW Save or SW Save register. The counter uses the G*i* DMA Read bit in the G*i* DMA Status register to tell the software which register to read. When G*i* DMA Read is 0, the most recent buffered counter value is in the HW Save register. When G*i* DMA Read is 1, the most recent buffered counter value is in the SW Save register.

Counter/Timer Functions and Examples

The GPCT provides counter/timer functions that are improved over those available on Am9513-based DAQ devices. Event counting, period measurement, pulse generation, and pulse-train generation are examples of existing counter/timer functions the NI-TIO supports. Enhancements to the existing counter/timer functions include quadrature encoder support and the ability to perform buffered-mode operations.

Event Counting

In event-counting functions, the counter counts events on the Selected Source input following the software arm. The software arm occurs when software sets the counter arm bit in the command register. The following actions are available in event counting:

- The Selected Source increments or decrements the counter.
- The Selected Gate indicates when to start and stop counting intervals or when to save the counter contents to the save register.
- The software either reads the counter value asynchronously from the G*i* Save register, or it reads the HW Save or SW Save register each time the hardware latches the counter value. In the latter case, interrupts notify the software that a save has occurred.
- AUX_LINE/UP_DOWN controls the direction of the counting.

Simple Event Counting

In simple event counting, the counter counts the number of pulses occurring on the Selected Source signal after the software arm. Software can read the counter contents at any time without disturbing the counting process. Figure 2-1 shows an example of simple event counting in which the counter counts five events on the Selected Source. The counter configuration is as follows:

- Source: external signal
- Gate: disabled
- Read from: SW Save register
- Direction: up

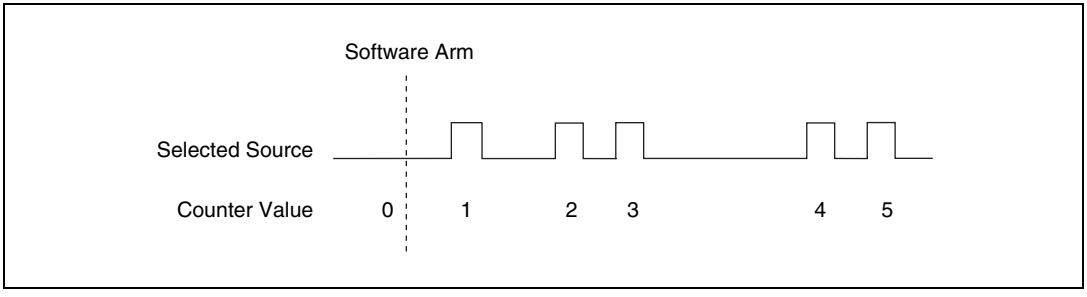

Figure 2-1. Simple Event Counting

Simple Gated-Event Counting

Simple gated-event counting is similar to simple event counting, but the counting process in simple gated-event counting is gated—halted and resumed—through the Selected Gate. When the Selected Gate is active, the counter counts pulses occurring on the Selected Source signal after the software arm. When the Selected Gate is inactive, the counter retains the current count value. Figure 2-2 shows an example of simple gated-event counting in which the gate action allows the counter to count only five of the pulses on the Selected Source. The counter configuration is as follows:

- Source: external signal
- Gate: external signal
- Read from: SW Save register
- Direction: up

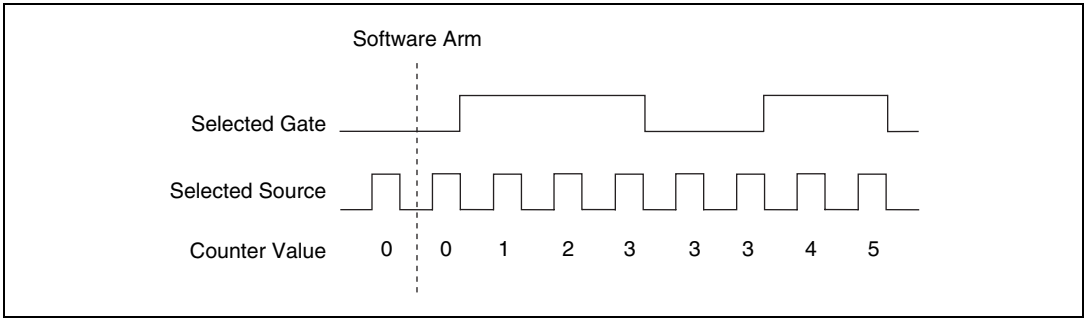

Figure 2-2. Simple Gated-Event Counting

Buffered Cumulative Event Counting

Buffered cumulative event counting is similar to simple event counting, but the Selected Gate signal in buffered cumulative event counting indicates when to save the counter value to the HW Save register. The active Selected Gate edge latches the count value into the HW Save register. Counting continues uninterrupted regardless of the Selected Gate activity. An interrupt notifies the CPU after each active Selected Gate edge so that the interrupt service routine can read the result from the HW Save register. Figure 2-3 shows cumulative event counting in which the gate action causes the HW Save register to save the counter contents twice. The counter configuration is as follows:

- Source: external signal
- Gate: external signal
- Trigger mode: gate ignored

- Interrupt on: DMA interrupt
- Read from: determined by G*i* DMA Status register
- Direction: up
- Load on gate: do not reload on gate

Caution Reading the value of a counter outside the interrupt service routine (ISR) may result in data loss.

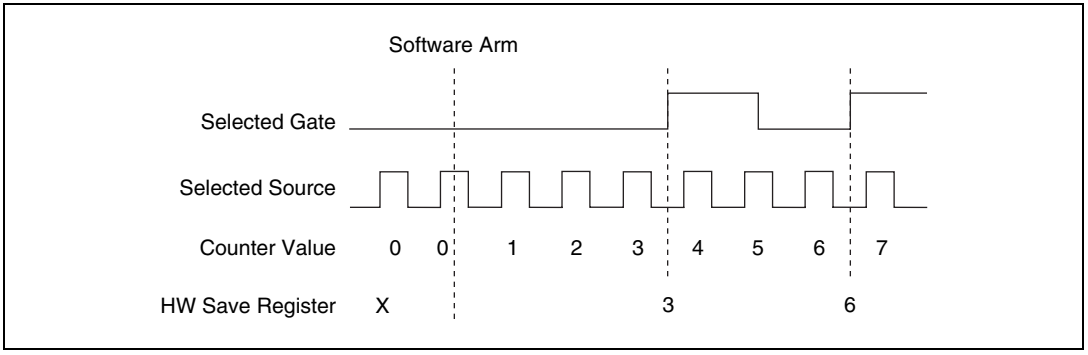

Figure 2-3. Cumulative Event Counting

Buffered Noncumulative Event Counting

Buffered noncumulative event counting is similar to simple event counting, but buffered noncumulative event counting has multiple counting intervals. The Selected Gate signal indicates the boundary between consecutive counting intervals. The counter counts the number of pulses occurring on the Selected Source signal after the software arm. Each active edge of the Selected Gate signal latches the count value for the current counting interval into either the HW Save or SW Save register and reloads the counter with the initial value to begin the next counting interval. An interrupt notifies the CPU after each counting interval so that the interrupt software can read the result from the HW Save register. Figure 2-4 shows buffered noncumulative event counting with two counting intervals. Three events are counted in each of the two counting intervals. The counter configuration is as follows:

- Source: external signal
- Gate: external signal
- Trigger mode: gate ignored
- Load on: gate

- Interrupt: on gate
- Read from: determined by G*i* DMA Status register
- Direction: up
- Load on gate: reload on gate

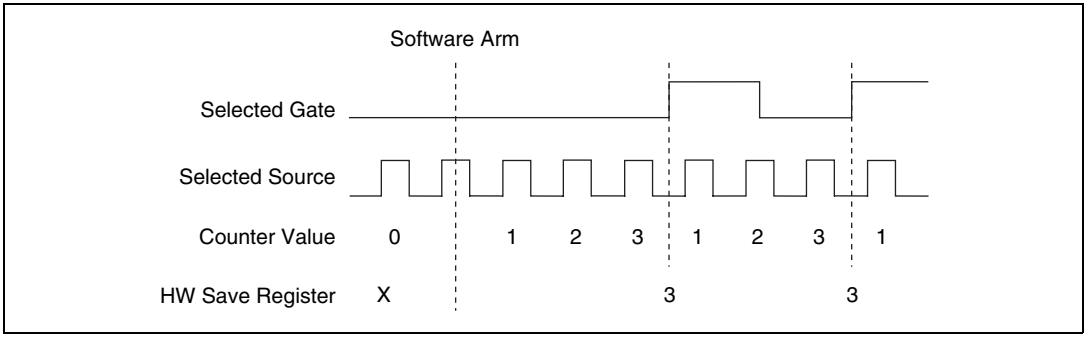

Figure 2-4. Buffered Noncumulative Event Counting

Position Measurement

In position measurement functions, the counter tracks the position of a quadrature encoder.

Relative Position Measurement

In relative position sensing, the counter tracks the relative position of the position encoder. Two types of events are possible: movement in the positive direction and movement in the negative direction. When Channel A leads Channel B, the counter increments. When Channel B leads Channel A, the counter decrements. The number of increments and decrements per cycle depends on the type of encoding: X1, X2, or X4. On NI-TIO counters, Channel A is hardwired to the default counter source pin, Channel B is hardwired to the AUX_LINE pin, and Channel Z is hardwired to the gate pin.

The software initially loads the counter with a value corresponding to the initial position of the object. Upon reaching terminal count (TC), the counter rolls over. You can obtain the relative object position at any time by asynchronously reading the counter value. Figure 2-5 shows an example of relative position sensing. The counter configuration is as follows:

- Encoder counting mode: X4
- Source select: internal timebase
- Read from: SW Save register

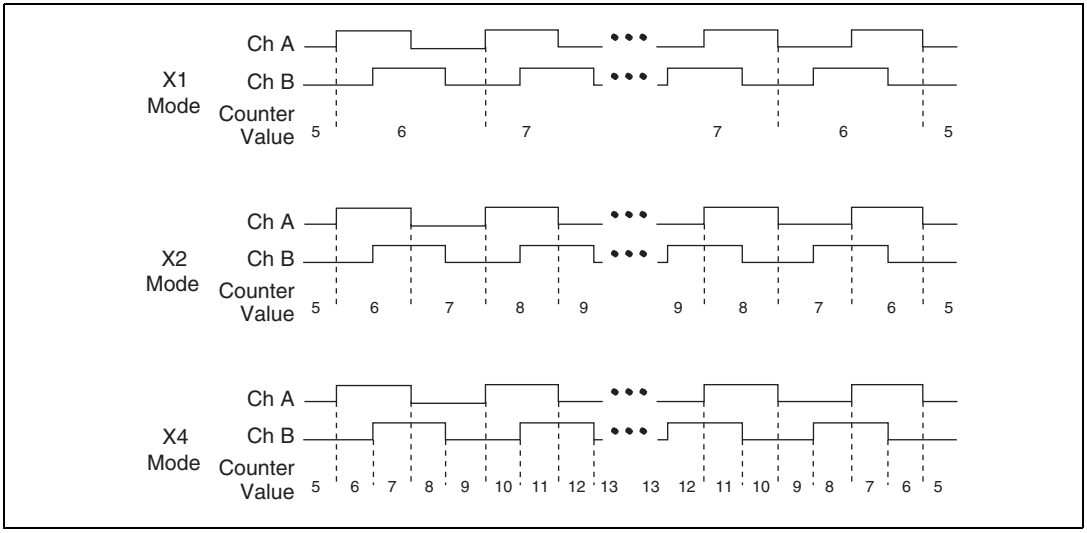

Figure 2-5. Relative Position Sensing

Time Measurement

In time measurement functions, the counter uses the Selected Source as a timebase to measure the time interval between events on the Selected Gate signal. The following actions are available in time measurement:

- Rising edges on the Selected Source can increment or decrement the counter during the measurement interval.
- Counting can begin and end on any two of the Selected Gate edges—rising, falling, or both.
- The HW Save register or the SW Save register can save the counter value upon completion of the measurement.

Single-Period Measurement

In single-period measurement, the counter uses the Selected Source to measure the period of the signal present on the Selected Gate input. The counter counts the number of rising edges occurring on the Selected Source between two active edges of the Selected Gate. At the completion of the period interval for the Selected Gate, the SW Save register contains the last counter value. Figure 2-6 shows a single-period measurement in which the period of the Selected Gate is five Selected Source rising edges.
The counter configuration is as follows:

- Source: internal clock
- Gate: external signal

- Gate mode: falling edge
- Second gate: selected gate
- Second gate mode: on
- Second gate polarity: non-inverted
- Count once: true

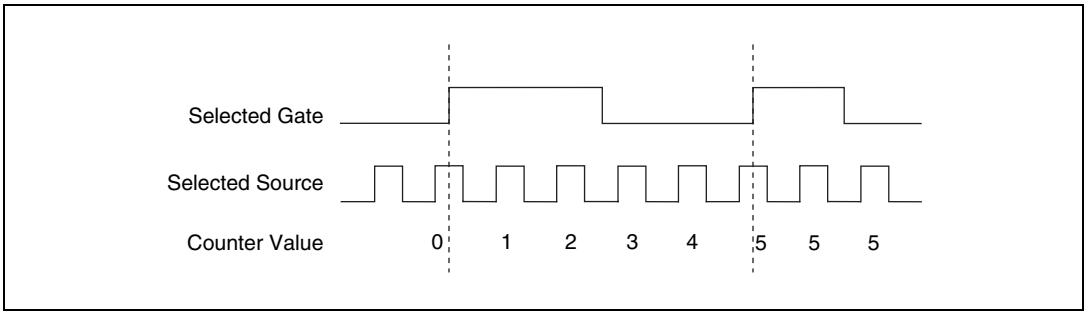

Figure 2-6. Single-Period Measurement

Single Pulse-Width Measurement

In single pulse-width measurement, the counter uses the Selected Source to measure the pulse width of the signal present on the Selected Gate input. The counter counts the number of rising edges occurring on the Selected Source while the Selected Gate signal remains in an active state. At the completion of the pulse-width interval for the Selected Gate, the SW Save register retains the counter value for software read. Figure 2-7 shows a single pulse-width measurement in which the pulse width of the Selected Gate is five Selected Source rising edges. The counter configuration is as follows:

- Source: internal
- Gate: external signal
- Gate mode: level
- Gate polarity: inverted
- Second gate: selected gate
- Second gate mode: on
- Second gate polarity: inverted
- Count once: true

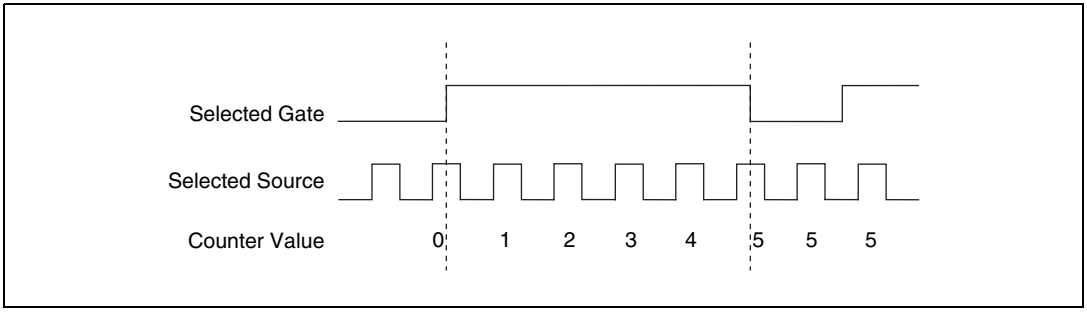

Figure 2-7. Single Pulse-Width Measurement

Buffered Period Measurement

Buffered period measurement is similar to single-period measurement, except that buffered period measurement takes measurements for multiple periods. The counter uses the Selected Source to measure the time interval between two active edges of the signal present on the Selected Gate input, counting the number of rising edges that occur on the Selected Source between each pair of active edges of the Selected Gate. At the completion of each period interval for the Selected Gate, the HW Save or SW Save register latches the counter value for software read. An interrupt notifies the CPU after each period so that the interrupt software can read the value in the HW Save register. Figure 2-8 shows two periods of a buffered period measurement in which the period is three Selected Source rising edges. The counter configuration is as follows:

- Source: internal clock
- Gate: external signal
- Gate mode: falling edge
- Second gate: selected gate
- Second gate mode: on
- Second gate polarity: non-inverted
- Read from: determined by G*i* DMA Status register
- Interrupt on: DMA interrupt
- Count once: false

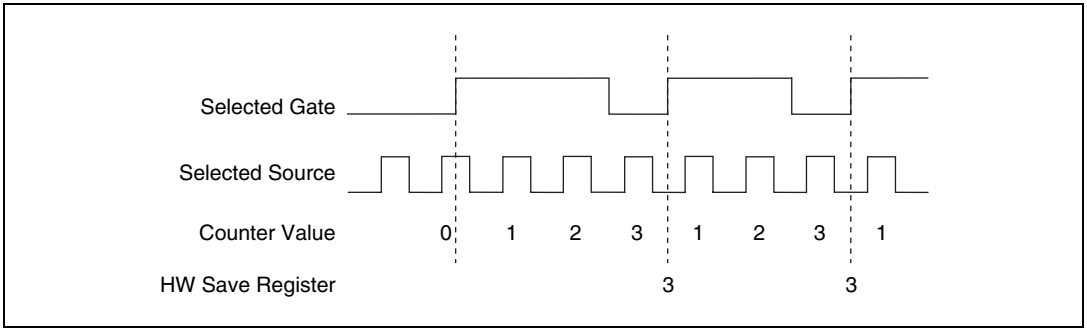

Figure 2-8. Buffered Period Measurement

Buffered Pulse-Width Measurement

Buffered pulse-width measurement is similar to single pulse-width measurement, but buffered pulse-width measurement takes measurements over multiple pulses. The counter uses the Selected Source to measure the pulse width of the signal present on the Selected Gate input, counting the number of rising edges that occur on the Selected Source while the Selected Gate remains in an active state. At the completion of each pulse-width interval for the Selected Gate, the HW Save or SW Save register latches the counter value for software read. An interrupt notifies the CPU after each period so that the interrupt software can read the value in the HW Save register. Figure 2-9 shows two pulse widths of a buffered pulse-width measurement in which the first pulse width is three Selected Source rising edges and the second pulse width is two Selected Source rising edges. The counter configuration is as follows:

- Source: internal
- Gate: external signal
- Gate mode: level
- Gate polarity: inverted
- Second gate: selected gate
- Second gate mode: on
- Second gate polarity: inverted
- Read from: determined by G*i* DMA Status register
- Interrupt on: DMA interrupt
- Count once: false

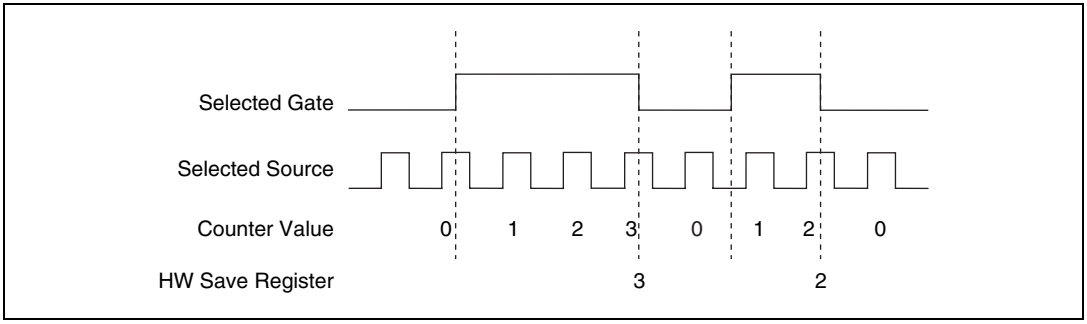

Figure 2-9. Buffered Pulse-Width Measurement

Pulse Generation

In pulse generation functions, the counter generates a single pulse of specified duration following the software arm. The software arm occurs when software sets the counter arm bit in the command register. The following actions are available in pulse generation:

- The counter uses the Selected Source as a timebase to generate the pulse.
- The user specifies the pulse parameters in terms of periods of the Selected Source input.
- The Selected Gate can serve as a trigger signal to generate a pulse after the first active gate edge or after each active gate edge.

Single Pulse Generation

The single pulse generation function generates a single pulse with programmable delay and programmable pulse width following the software arm. Because the counter uses the Selected Source as a timebase to generate the pulse, specify the pulse parameters in terms of periods of the Selected Source input. Software implements pulse generation by loading the delay value into the counter, loading the pulse-width value into the load register, and programming the counter output G_OUT to change states on counter terminal count (TC). Figure 2-10 shows the generation of a single pulse with a pulse delay of four and a pulse width of three. The counter configuration is as follows:

- Source: internal
- Gate: none
- Output mode: toggle on TC
- Direction: down

- Count once: true
- Load on: TC

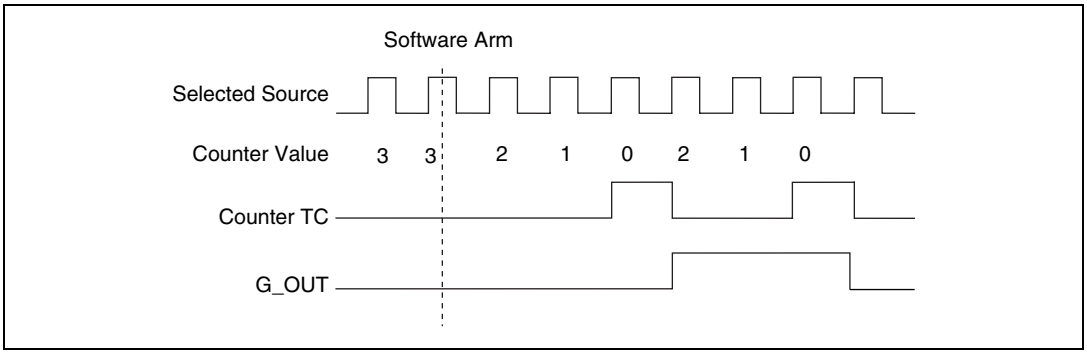

Figure 2-10. Single Pulse Generation

Pulse-Train Generation

In the pulse-train generation functions, the counter generates a continuous stream of pulses of specified interval and duration following the software arm and an optional hardware trigger. The software arm occurs when software sets the counter arm bit in the NI-TIO register. The following actions are available in pulse-train generation:

- The pulse parameters can be specified in terms of periods of the Selected Source input.
- The Selected Gate input can serve as a trigger signal to generate a stream of pulses only after the active gate edge occurs.

Continuous Pulse-Train Generation

This function generates a sequence of pulses with programmable pulse interval and pulse width. Because the counter uses the Selected Source as a timebase to generate the pulses, specify the programmable parameters in terms of periods of the Selected Source input. Pulse-train generation is implemented in software by loading the pulse parameters into the counter and load registers, and by programming the counter to switch load registers on every counter TC. Figure 2-11 shows the generation of three pulses with a delay from trigger of three, a pulse interval of four, and a pulse width of three. The counter configuration is as follows:

- Source: internal
- Gate: none
- Output mode: toggle on TC

- Direction: down
- Count once: false
- Load on: TC
- Trigger mode: only gate edge starts
- Reload source switching: true

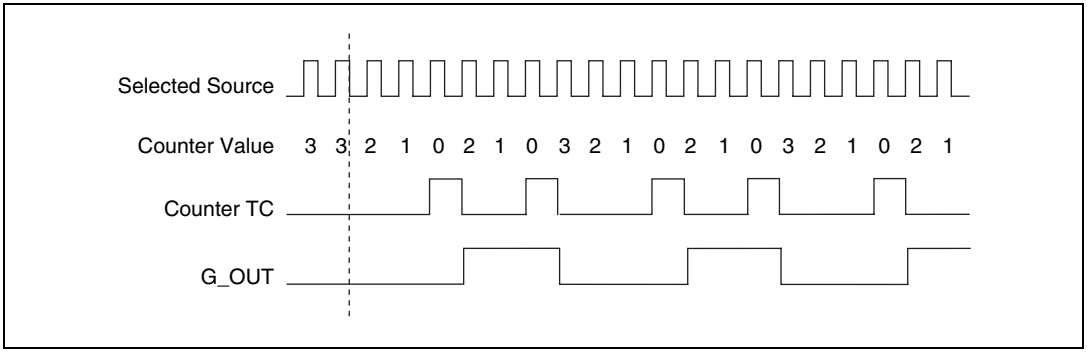

Figure 2-11. Continuous Pulse-Train Generation

Single Triggered Pulse Generation

Single triggered pulse generation is similar to single pulse generation, the Selected Gate in single triggered pulse generation provides a trigger function. An active Selected Gate edge following the software arm causes the counter to generate a single pulse with programmable delay and programmable pulse width. Specify the programmable parameters in terms of periods of the Selected Source input. Single triggered pulse generation is implemented in software by loading the delay value into the counter, loading the pulse-width value into the load register, programming the counter output G_OUT to change states on counter TC, and configuring the Selected Gate as the trigger signal. Figure 2-12 shows the generation of a single pulse with a pulse delay of four and a pulse width of three. The counter configuration is as follows:

- Source: internal
- Gate: external signal
- Output mode: toggle on TC
- Direction: down
- Count once: true
- Load on: TC
- Trigger mode: gate edge only starts

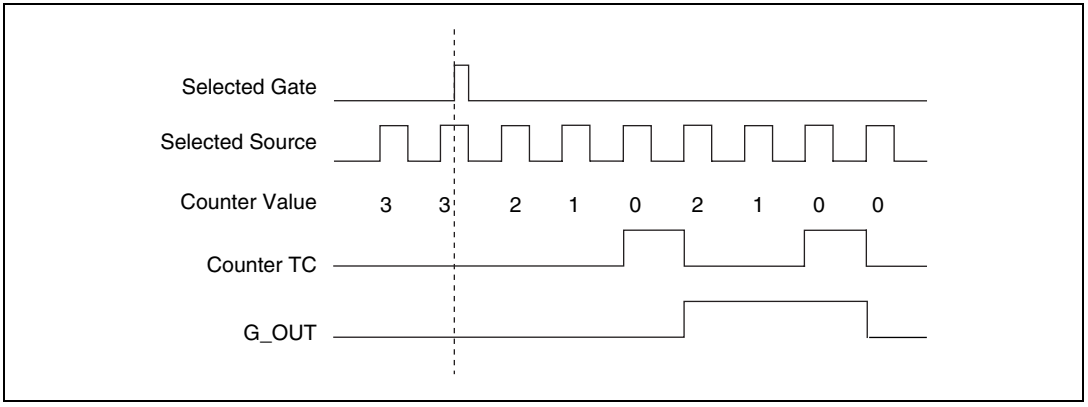

Figure 2-12. Single Triggered-Pulse Generation

3

Register Maps

This chapter contains NI-TIO and MITE register maps and register descriptions.

NI-TIO

The NI-TIO (0) location is PCI Buffer Address Register (BAR) 1, offset 0x0. The NI-TIO (1) location on the 6602 and 6608 devices is PCI BAR1, offset 0x800.

Register Map and Descriptions

This section includes a register map and a bit-by-bit description of each register in the NI-TIO. Table 3-1 provides the register name, the register address offset from the device base address (BAR1), the type of register—read-only and write-only, and the size of the register in bits. Registers are grouped in the table by offset, and the register descriptions following the table are organized alphabetically.

Table 3-1. TIO Register Address Map

Register Name	Offset (Hex)	Type	Size
G0 Interrupt Acknowledge	0x004	Write-only	16-bit
G0 Status Register	0x004	Read-only	16-bit
G1 Interrupt Acknowledge	0x006	Write-only	16-bit
G1 Status Register	0x006	Read-only	16-bit
G01 Status Register	0x008	Read-only	16-bit
G0 Command Register	0x00C	Write-only	16-bit
G1 Command Register	0x00E	Write-only	16-bit
G0 HW Save Register	0x010	Read-only	32-bit
G1 HW Save Register	0x014	Read-only	32-bit
G0 SW Save Register	0x018	Read-only	32-bit

Table 3-1. TIO Register Address Map (Continued)

Register Name	Offset (Hex)	Type	Size
G1 SW Save Register	0x01C	Read-only	32-bit
G0 Mode Register	0x034	Write-only	16-bit
G01 Joint Status 1 Register	0x036	Read-only	16-bit
G1 Mode Register	0x036	Write-only	16-bit
G0 Load A Register	0x038	Write-only	32-bit
G01 Joint Status 2 Register	0x03A	Read-only	16-bit
G0 Load B Register	0x03C	Write-only	32-bit
G1 Load A Register	0x040	Write-only	32-bit
G1 Load B Register	0x044	Write-only	32-bit
G0 Input Select Register	0x048	Write-only	16-bit
G1 Input Select Register	0x04A	Write-only	16-bit
G01 Joint Reset Register	0x090	Write-only	16-bit
G0 Interrupt Enable	0x092	Write-only	16-bit
G1 Interrupt Enable	0x096	Write-only	16-bit
G0 Counting Mode Register	0x0B0	Write-only	16-bit
G1 Counting Mode Register	0x0B2	Write-only	16-bit
G0 Second Gate Register	0x0B4	Write-only	16-bit
G1 Second Gate Register	0x0B6	Write-only	16-bit
G0 DMA Config Register	0x0B8	Write-only	16-bit
G0 DMA Status Register	0x0B8	Read-only	16-bit
G1 DMA Config Register	0x0BA	Write-only	16-bit
G1 DMA Status Register	0x0BA	Read-only	16-bit
G2 Interrupt Acknowledge	0x104	Write-only	16-bit
G2 Status Register	0x104	Read-only	16-bit
G3 Interrupt Acknowledge	0x106	Write-only	16-bit

Table 3-1. TIO Register Address Map (Continued)

Register Name	Offset (Hex)	Type	Size
G3 Status Register	0x106	Read-only	16-bit
G23 Status Register	0x108	Read-only	16-bit
G2 Command Register	0x10C	Write-only	16-bit
G3 Command Register	0x10E	Write-only	16-bit
G2 HW Save Register	0x110	Read-only	32-bit
G3 HW Save Register	0x114	Read-only	32-bit
G2 SW Save Register	0x118	Read-only	32-bit
G3 SW Save Register	0x11C	Read-only	32-bit
G2 Mode Register	0x134	Write-only	16-bit
G23 Joint Status 1 Register	0x136	Read-only	16-bit
G3 Mode Register	0x136	Write-only	16-bit
G2 Load A Register	0x138	Write-only	32-bit
G23 Joint Status 2 Register	0x13A	Read-only	16-bit
G2 Load B Register	0x13C	Write-only	32-bit
G3 Load A Register	0x140	Write-only	32-bit
G3 Load B Register	0x144	Write-only	32-bit
G2 Input Select Register	0x148	Write-only	16-bit
G3 Input Select Register	0x14A	Write-only	16-bit
G23 Joint Reset Register	0x190	Write-only	16-bit
G2 Interrupt Enable	0x192	Write-only	16-bit
G3 Interrupt Enable	0x196	Write-only	16-bit
G2 Counting Mode Register	0x1B0	Write-only	16-bit
G3 Counting Mode Register	0x1B2	Write-only	16-bit
G3 Second Gate Register	0x1B6	Write-only	16-bit
G2 Second Gate Register	0x1B4	Write-only	16-bit

Table 3-1. TIO Register Address Map (Continued)

Register Name	Offset (Hex)	Type	Size
G2 DMA Config Register	0x1B8	Write-only	16-bit
G2 DMA Status Register	0x1B8	Read-only	16-bit
G3 DMA Config Register	0x1BA	Write-only	16-bit
G3 DMA Status Register	0x1BA	Read-only	16-bit
Clock Config Register	0x73C	Write-only	32-bit

Clock Config Register

Address Offset: 0x73C
Type: Write
Size: 32-bit
Bit Map:

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0

23	22	21	20	19	18	17	16
0	0	Counter Swap	0	0	0	0	0

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit	Name	Description
21	Counter Swap	Setting this bit swaps the dedicated counter pins (SRC, GATE, UP/DOWN, OUT) between counter locations 0 through 3 and 4 through 7. This setting allows two NI-TIO ASICs to be configured to use all eight dedicated counter locations. The addressing of the counters remains the same. This setting also applies to dedicated pins, such as the Quadrature and Output. The mapping is as follows: 0 <-> 4 1 <-> 5 2 <-> 6 3 <-> 7

G*i* Command Register

Address Offsets: 0x00C (G0), 0x00E (G1), 0x10C (G2), 0x10E (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G*i* Disarm Copy	G*i* Save Trace Copy	G*i* Arm Copy	G*i* Bank Switch Enable	G*i* Bank Switch Mode	G*i* Bank Switch Start	G*i* Little Big Endian	G*i* Synchronized Gate

7	6	5	4	3	2	1	0
G*i* Write Switch	G*i* Up/ Down 1	G*i* Up/ Down 0	G*i* Disarm	0	G*i* Load	G*i* Save Trace	G*i* Arm

Bits	Name	Description
15	G*i* Disarm Copy	Setting this bit disarms the other counter in the pair. The copy bits allow a single write to perform a command on both counters in the pair.
14	G*i* Save Trace Copy	This bit controls the SW Save register. When G*i* Save Trace Copy is clear, the SW Save register is open and tracing the counter. When set, the SW Save register goes into the latched mode after the next clock edge to assure valid data was latched. The latching process is complete when G*i* Save is set. The copy bits allow a single write to perform a command on both counters in the pair.
13	G*i* Arm Copy	Setting this bit arms the other counter in the pair. The counter remains armed until disabled in hardware or by G*i* Disarm Copy.
12	G*i* Bank Switch Enable	Setting this bit enables bank switching. When the counter is armed, this bit enables switching between the two banks of A and B Load registers, referred to as X and Y. If the counter is disarmed, this bit selects the bank written when accessing the Load A and Load B registers.

0—Writes Bank X
1—Writes Bank Y

11 G*i* Bank Switch Mode

If bank switching is enabled, this bit selects the source that causes a bank switch to occur during operation.

0—Gate
1—Software

10 G*i* Bank Switch Start

Setting this bit causes a bank switch on the condition determined by Bank Switch Mode. The bit automatically clears after the bank switch.

9 G*i* Little Big Endian

When using automatic interrupt acknowledgement, the G*i* Little Big Endian bit determines which segment of the load or save register triggers the acknowledgement.

0—Low register, bits 15–0
1—High register, bits 31–16

8 G*i* Synchronize Gate

Setting this bit synchronizes the GATE signal to the counter clock. This bit should be enabled, unless the gate signal is definitely synchronized to the SRC and there is sufficient setup time.

7 G*i* Write Switch

This setting automatically directs load register writes to the inactive bank. When the bit is clear, writes to Load A always change A. When the bit is set, writes to Load A are directed to the inactive bank.

6–5 G*i* Up/Down This bit determines the counting direction.

00—Always down
01—Always up
10—Hardware selected based on the UP/DOWN I/O pin: 0 = down, 1 = up
11—Hardware selected based on the internal GATE, 0 = down, 1 = up

4 G*i* Disarm Setting this bit disarms the counter.

2	G*i* Load	This strobe bit uses software to load the initial counter value. When the bit is asserted, the selected load register (A or B) transfers to the counter.
1	G*i* Save Trace	This bit controls the SW Save register. When Gi Save Trace is clear, the SW Save register is open and tracing the counter. When set, the SW Save register goes into the latched mode after the next clock edge to assure valid data was latched. The latching process is complete when G*i* Save is set.
0	G*i* Arm	Setting this bit arms the counter. The counter remains armed until disabled in hardware or by G*i* Disarm.

G*i* Counting Mode Register

Address Offsets: 0x0B0 (G0), 0x0B2 (G1), 0x1B0 (G2), 0x1B2 (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	G*i* Alternate Sync	G*i* Prescale	0	0	0	0

7	6	5	4	3	2	1	0
0	G*i* Index Phase 1	G*i* Index Phase 0	G*i* Index Mode	0	G*i* Counting Mode 2	G*i* Counting Mode 1	G*i* Counting Mode 0

Bits	Name	Description
13	G*i* Alternate Sync	Alternate Synchronization. When synchronizing a signal, the NI-TIO uses the falling edge of the clock when an internal timebase is chosen. For other signals, the clock may free run, in which case the selected source synchronizes the signal, and a delayed version clocks the counter. Setting the G*i* Alternate Sync bit adds an additional synchronization bit to the NI-TIO. When set, the rising source edge synchronizes the signal and clocks the counter, which gives a full state of setup and delays the reaction one clock. This mode must be enabled if the counter is clocked above 40 MHz, including cases in which TIMEBASE 3 is implicitly selected, such as in synchronous counting and quadrature modes.
12	G*i* Prescale	When this bit is enabled, the high-speed counter divides the selected source by eight before clocking the counter. This mode allows signal frequency to be measured, even when the frequency is above the 80 MHz limit for the counters.

6–5	G*i* Index Phase	The index phase field determines the state of the A and B quadrature signals and is where the index, or Z signal, is acted upon. The Z index can span multiple phases of the quadrature, but it is recommended that you reload the counter in only one of the phases. 00—A low, B low 01—A low, B high 10—A high, B low 11—A high, B high
4	G*i* Index Mode	Index mode affects the new counting modes in the following ways: Quadrature mode—The Z input signal, or index, can reload the counter in a particular phase. The counter reloads when this bit is set, A and B match the index phase, and the Z input is high. Two-pulse mode—The counter reloads while Z is loaded. Source synchronous mode—Setting this bit disables the edge detector on the source signal that requires it to be synchronous.
2–0	G*i* Counting Mode	This field adds counting modes to the NI-TIO GPCT for interfacing to encoders and other new applications. 000—One. Normal counting mode. 001—Quadrature Mode X1. This mode allows direct interfacing to quadrature encoders for position and velocity measurement. The encoder has two and sometimes three signals: signal A connects to the dedicated source pin of the counter; signal B connects to the UP/DOWN pin; and signal Z connects to the GATE pin. Signals A and B pulse with each movement and are 90 degrees out of phase to indicate direction. The Z signal reloads the counter when Index Mode is enabled. The X1 mode increments or decrements the counter once per total phase.

010—Quadrature Mode X2. This mode counts on both edges of the A signal. Two counts per cycle are recorded.

011—Quadrature Mode X4. This mode counts on both edges of the A and B signals. Four counts per cycle are recorded.

100—Two-Pulse Mode. In this mode, a rising edge on the A signal increments the counter, and a rising edge on the B signal decrements the counter. The counter reloads while the Z signal is high and enabled.

110—Synchronous Source Mode. Several counter features, such as hardware save and load, depend on source edges to operate. However, it is sometimes necessary to measure event rates down to 0 Hz. Synchronous Source Mode runs the counter at maximum timebase, but enables it on a source edge to mimic running off that source while providing a free-running clock.

G*i* DMA Config Register

Address Offsets: 0x0B8 (G0), 0x0BA (G1), 0x1B8 (G2), 0x1BA (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	0	0	0	0	G*i* DMA Int	G*i* DMA Write	G*i* DMA Enable

Bits	Name	Description
2	G*i* DMA Int	Direct Memory Access Interrupt. This bit uses DMA mode to implement PIO operations. When set, the counter interrupt asserts with the counter DRQ signal, indicating that service is needed. If reading data, the software reads either the HW Save or SW Save register, as determined by the G*i* Read Bank bit. Write data to the appropriate A or B register.
1	G*i* DMA Write	Direct Memory Access Write. This bit indicates the direction of the DMA operation. 0—DMA controller reads data from the NI-TIO save registers 1—DMA controller writes data to the NI-TIO load registers
0	G*i* DMA Enable	Direct Memory Access Enable. When this bit is set, the NI-TIO adds a new DMA mode for streaming counts into or out of the counters. The read mode uses both the hardware and the SW Save registers as a two-element FIFO in order to increase the rate at which pulse or period measurements are made. When using a DMA controller (asserted DACK), the DACK reads are automatically routed to the proper register, and data is alternately stored

on gate edges. When using PIO, the G*i* Read Bank bit indicates the register at the head of the FIFO.

For pulse generation, DMA can reload the load register when a bank switch occurs. DRQ asserts on the bank switch and clears when the last load register is written. G*i* Write Switch and G*i* Little Big Endian determine the last load register. If G*i* Write Switch is clear, writes are directed to Load B, and DRQ clears on a write to the half of Load B as determined by G*i* Little Big Endian. If G*i* Write Switch is true, the first write goes to Load B, DRQ remains asserted, and the second write goes to Load A, which clears DRQ.

G*i* DMA Status Register

Address Offsets: 0x0B8 (G0), 0xBA (G1), 0x1B8 (G2), 0x1BA (G3)

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G*i* DRQ Status	G*i* DRQ Error	G*i* DMA Readbank	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Bits	Name	Description
15	G*i* DRQ Status	DMA Request Status. This bit is set when the counter needs DMA service and clears automatically when the request is serviced.
14	G*i* DRQ Error	DMA Request Error. This bit is set when a DMA overflow error occurs on a read operation and when an underflow error occurs on a write operation. When reading, this bit sets if a save request occurs when the FIFO is full and another DMA read follows. The save request does not corrupt the data when the FIFO is received after completion. When writing, an error is set if the bank switches while DRQ is still set, which indicates that the two switches occurred before the load registers were serviced.
13	G*i* DMA Readbank	When implementing the PIO for read DMA, the DMA Readbank indicates which save register contains the next data to be transferred. This bit alternates with each read. 0—HW save 1—SW save

G*i* Input Select Register

Address Offsets: 0x048 (G0), 0x04A (G1), 0x148 (G2), 0x14A (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G*i* Source Polarity	G*i* Output Polarity	G*i* OR Gate	G*i* Gate Select Load Source	G*i* Gate Select 4	G*i* Gate Select 3	G*i* Gate Select 2	G*i* Gate Select 1

7	6	5	4	3	2	1	0
G*i* Gate Select 0	G*i* Source Select 4	G*i* Source Select 3	G*i* Source Select 2	G*i* Source Select 1	G*i* Source Select 0	0	0

Bits	Name	Description
15	G*i* Source Polarity	Set this bit to invert the selected source signal, changing the polarity of the active edge.
14	G*i* Output Polarity	Set this bit to invert the counter output signal.
13	G*i* OR Gate	Set this bit to OR the output of the adjacent counter with the selected gate. When the counter is not counting, only the adjacent counter output is the gate. Clearing this bit removes the effect on the gate.
12	G*i* Gate Select Load Source	When this bit is set, the selected gate signal chooses the load source for the counter. An active gate level chooses Load A, while an inactive level chooses Load B. The G*i* Gating mode must be set to Level mode.
11–7	G*i* Gate Select <4..0>	This bit selects the signal to serve as the gate for the counter.

0—Source Pin *i*; the source pin dedicated to this counter

1—Gate Pin *i*; the gate pin dedicated to this counter
2—Gate Pin 0, I/O Pin 38
3—Gate Pin 1, I/O Pin 34
4—Gate Pin 2, I/O Pin 30
5—Gate Pin 3, I/O Pin 26
6—Gate Pin 4, I/O Pin 22
7—Gate Pin 5, I/O Pin 18
8—Gate Pin 6, I/O Pin 14
9—Gate Pin 7, I/O Pin 10
10—Next Src; the selected source of the adjacent counter
11—RTSI 0
12—RTSI 1
13—RTSI 2
14—RTSI 3
15—RTSI 4
16—RTSI 5
17—RTSI 6
20—Next Out; the counter of the adjacent counter
30—Logic low
31—Logic low

6–2 G*i* Source Select <4..0>

This bit selects the signal the counter uses as the source.

0—Timebase 1; the internal timebase (20 MHz)
1—Source Pin *i*; the source pin dedicated to this counter
2—Source Pin 0, I/O Pin 39
3—Source Pin 1, I/O Pin 35
4—Source Pin 2, I/O Pin 31
5—Source Pin 3, I/O Pin 27
6—Source Pin 4, I/O Pin 23
7—Source Pin 5, I/O Pin 19
8—Source Pin 6, I/O Pin 15
9—Source Pin 7, I/O Pin 11
10—Next Gate; the selected gate of the adjacent counter
11—RTSI 0
12—RTSI 1
13—RTSI 2
14—RTSI 3
15—RTSI 4
16—RTSI 5
17—RTSI 6

18—Timebase 2; the internal timebase (100 KHz)
19—Next TC; the adjacent counter's terminal count
30—Timebase 3; the internal timebase (the maximum frequency)
31—Logic low

G0 Interrupt Enable
G2 Interrupt Enable

Address Offsets: 0x092 (G0), 0x192 (G2)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	G0 TC Interrupt Enable	0	0	0	0	0	0

Bit	Name	Description
6	G0 TC Interrupt Enable	G0 Terminal Count Interrupt Enable. Setting this bit allows a terminal count interrupt to assert the counter interrupt.

G1 Interrupt Enable
G3 Interrupt Enable

Address Offsets: 0x096 (G1), 0x196 (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	G1 TC Interrupt Enable	0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit	Name	Description
9	G1 TC Interrupt Enable	G1 Terminal Count Interrupt Enable. Setting this bit allows a terminal count interrupt to assert the counter interrupt.

G*i* Load A Register

Address Offsets: 0x038 (G0), 0x040 (G1), 0x138 (G2), 0x140 (G3)

Type: Write

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
Load A.31	Load A.30	Load A.29	Load A.28	Load A.27	Load A.26	Load A.25	Load A.24

23	22	21	20	19	18	17	16
Load A.23	Load A.22	Load A.21	Load A.20	Load A.19	Load A.18	Load A.17	Load A.16

15	14	13	12	11	10	9	8
Load A.15	Load A.14	Load A.13	Load A.12	Load A.11	Load A.10	Load A.9	Load A.8

7	6	5	4	3	2	1	0
Load A.7	Load A.6	Load A.5	Load A.4	Load A.3	Load A.2	Load A.1	Load A.0

Bits	Name	Description
31–0	Load A.<31..0>	The Load A field is for loading the counter with G*i* Load, or for reloading on gate or TC conditions. This field can alternate with Load B by using Reload Source Switching. The A and B registers are actually two banks of load registers, X and Y, which are controlled by the bank switching attributes in the G*i* Command register.

G*i* Load B Register

Address Offsets: 0x03C (G0), 0x044 (G1), 0x13C (G2), 0x144 (G3)

Type: Write

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
Load B.31	Load B.30	Load B.29	Load B.28	Load B.27	Load B.26	Load B.25	Load B.24

23	22	21	20	19	18	17	16
Load B.23	Load B.22	Load B.21	Load B.20	Load B.19	Load B.18	Load B.17	Load B.16

15	14	13	12	11	10	9	8
Load B.15	Load B.14	Load B.13	Load B.12	Load B.11	Load B.10	Load B.9	Load B.8

7	6	5	4	3	2	1	0
Load B.7	Load B.6	Load B.5	Load B.4	Load B.3	Load B.2	Load B.1	Load B.0

Bits	Name	Description
31–0	Load B.<31..0>	The Load B field is for loading the counter with G*i* Load, or for reloading on gate or TC conditions. It can alternate with Load B by using Reload Source Switching in the G*i* Mode register. The A and B registers are actually two banks of load registers, X and Y, which are controlled by the bank switching attributes in the G*i* Command register.

G*i* Mode Register

Address Offsets: 0x034 (G0), 0x036 (G1), 0x134 (G2), 0x136 (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G*i* Reload Source Switching	G*i* Loading on Gate	G*i* Gate Polarity	G*i* Loading on TC	G*i* Counting Once 1	G*i* Counting Once 0	G*i* Output Mode 1	G*i* Output Mode 0

7	6	5	4	3	2	1	0
G*i* Load Source Select	G*i* Stop Mode 1	G*i* Stop Mode 0	G*i* Trigger Mode for Edge Gate 1	G*i* Trigger Mode for Edge Gate 0	G*i* Gate on Both Edges	G*i* Gating Mode	G*i* Gating Mode

Bits	Name	Description
15	G*i* Reload Source Switching	When G*i* Gate Select Load Source is 0, the G*i* Reload Source Switching bit determines if the reloading always comes from the same load register (0), or if it alternates between the two (1).
14	G*i* Loading on Gate	When this bit is set, the gate edge reloads the counter on the next source edge. Set the G*i* Trigger Mode for Edge Gate to 3 to reload the counter on each selected edge. Otherwise, the counter reloads on the gate that stops the counter. You can also use G*i* Loading on Gate with G*i* Loading on TC.
13	G*i* Gate Polarity	Setting the bit inverts the gate signal, making it active low rather than the normal active high.
12	G*i* Loading on TC	Loading on Terminal Count. If this bit is clear, the counter rolls over when it reaches TC. When set, the counter reloads from a Load register on TC. You can also use G*i* Loading on TC with G*i* Loading on Gate.

11, 10 G*i* Counting Once

This field determines whether the counter disarms when the counter stops for a hardware condition.

00—No hardware disarm
01—Disarm at the TC that stops counting
10—Disarm at the gate that stops counting
11—Disarm at the first TC or gate that stops counting

9, 8 G*i* Output Mode

G*i* Output Mode determines the counter output type.

00—Reserved
01—The counter TC is the output; it asserts for one clock at TC
10—Output toggles value on each TC
11—Output toggles on TC or gate

7 G*i* Load Source Select

When the counter is disarmed, this bit determines which load register—Load A (0) or Load B (1)—loads the counter in response to a G*i* Load. Once the counter is armed, the G*i* Reload Source Switching bit determines the load source. After the counter is armed, writing this bit has no effect.

6, 5 G*i* Stop Mode This bit determines the mode in which the hardware stops the counter.

00—Stop on gate condition
01—Stop on gate or first TC
10—Stop on gate or second TC
11—Reserved

Note To make these conditions TC only, use G*i* Trigger Mode for Edge Gate to turn off the edge gate stopping.

4, 3 G*i* Trigger Mode for EdgeGate

This field determines how a gate edge affects the counting when gating is enabled.

00—The first gate edge starts, and the next gate edge stops the counting.
01—The first gate edge stops, and the second gate edge starts the counting.

10—The gate edge that always starts the counting. TC normally stops this mode.
11—The gate not used for starting or stopping. This gate may still save, reload, or load select. Selections 0 and 1 are valid when G*i* Stop Mode is 0, and selection 0 through 2 are only valid for edge gating and level gating.

2 G*i* Gate on Both Edges

When G*i* Gate on Both Edges is set and G*i* Gating Mode is set to rising mode, the edge gating modes operate on both the rising and falling edges.

1, 0 G*i* Gating Mode

This field determines how the gate signal is interpreted for gating operations.

00—Gating disabled
01—Level gating
10—Rising edge gating
11—Falling edge gating

Note G*i* Gate Polarity can change the edge for modes 2 and 3. When gating is disabled, you can use the gate for counting direction only.

G01 Joint Reset Register
G23 Joint Reset Register

Address Offsets: 0x090 (G01), 0x190 (G23)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
0	0	0	0	G1 Reset	G0 Reset	0	0

Bits	Name	Description
3–2	G*i* Reset	Writing this strobe bit to 1 resets the counter. This bit automatically clears, and the counter is disarmed.

G*i* Second Gate Register

Address Offsets: 0x0B4 (G0), 0x0B6 (G1), 0x1B4 (G2), 0x1B6 (G3)

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
0	0	G*i* Second Gate Polarity	0	G*i* Second Gate Select 4	G*i* Second Gate Select 3	G*i* Second Gate Select 2	G*i* Second Gate Select 1

7	6	5	4	3	2	1	0
G*i* Second Gate Select 0	0	0	0	0	0	0	G*i* Second Gate Mode

Bits	Name	Description
13	G*i* Second Gate Polarity	Setting this bit inverts the selected second gate, changing the polarity.
11–7	G*i* Second Gate Select <4..0>	This field selects the signal used as the second gate for the counter. 0—Source Pin *i*; the source pin dedicated to this counter 1—Up/Down Pin *i*; the Up/Down pin dedicated to this counter 2—Up/Down Pin 0, I/O Pin 37 3—Up/Down Pin 1, I/O Pin 33 4—Up/Down Pin 2, I/O Pin 29 5—Up/Down Pin 3, I/O Pin 25 6—Up/Down Pin 4, I/O Pin 21 7—Up/Down Pin 5, I/O Pin 17 8—Up/Down Pin 6, I/O Pin 13 9—Up/Down Pin 7, I/O Pin 9 10—Next Src; the adjacent counter's selected source 11—RTSI 0 12—RTSI 1 13—RTSI 2

14—RTSI 3
15—RTSI 4
16—RTSI 5
17—RTSI 6
20—Next Out; the adjacent counter's output
30—Selected gate; the output of the gate selection, and not the selected gate I/O pin. For example, if the gate is set to (1) Gate Pin *i* and if G*i* Output Polarity is set, the alternate gate is an inverted Gate Pin *i* signal. This gate is useful for pulse measurement.
31—Logic low

0 G*i* Second Gate Mode

The second gate feature allows one signal to start the counter and another to stop it for two-edge separation measurements. When set, G*i* Second Gate Mode modifies the actual gate signal with a combination of the first and second gate. An assertion of the second gate signals asserts the counter gate, and an assertion of the gate signal deasserts the gate. You can then use this new gate signal for start and stop operations.

G*i* Second Gate Mode is also useful in pulse-width measurements. The level gating mode starts counting if the counter is armed while the gate is high, so the first measurement may be too short. Using the selected gate input to the second gate and inverting both gate and second gate polarity forces a rising edge to occur before the gate asserts. As a result, the first pulse is measured.

G*i* Second Gate Mode is also used for two-edge separation measurements.

G*i* Status Register

Address Offsets: 0x004 (G0), 0x006 (G1), 0x104 (G2), 0x106 (G3)

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Gi Interrupt	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	Gi TC Status	X	X	X

Bits	Name	Description
15	G*i* Interrupt	This counter asserts an interrupt. TC, GATE, or DMA Interrupt is true and enabled.
3	G*i* TC Status	Terminal Count Status. This bit indicates that the counter has reached terminal count. Setting G*i* TC Interrupt Ack clears this bit. TC Status is useful for generating interrupts at a constant frequency.

G01 Status Register

Address Offset: 0x008

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G1 Gate Error	G0 Gate Error	G1 TC Error	G0 TC Error	G1 No Load Between Gates	G0 No Load Between Gates	G1 Armed	G0 Armed

7	6	5	4	3	2	1	0
G1 Stale Data	G0 Stale Data	G1 Next Load Source	G0 Next Load Source	G1 Counting	G0 Counting	G1 Save	G0 Save

Bits	Name	Description
15–14	G*i* Gate Error	G*i* Gate Error sets when a second gate interrupt is detected before the previous one has been acknowledged. G*i* Gate Error Confirm clears this bit.
13–12	G*i* TC Error	Terminal Count Error. This bit sets when two terminal count interrupts occur without an acknowledgment. G*i* TC Error Confirm clears this bit.
11–10	G*i* No Load Between Gates	This bit indicates that a load did not occur between the selected gate edges. G*i* Load or G*i* Reset clears this bit.
9–8	G*i* Armed	This bit sets when the counter is armed.
7–6	G*i* Stale Data	This error bit sets if two relevant GATE edges occur without a SRC edge between them. Because reaction to GATE edges depends on the SRC edges, it may have generated incorrect data. The synchronous counting mode is one way to prevent this error. In this mode, the Stale bit updates on each GATE edge and reflects the state of the HW Save register. The Permanent Stale Data bit, located

		in the Joint Status 2 register, records the error until it is cleared.
5–4	G*i* Next Load Source	This bit indicates which load bank to load from next. 0—Load register A 1—Load register B
3–2	G*i* Counting	G*i* Counting is asserted when the counter is armed and enabled for counting. It reflects the state of the terms used for GATE or TC disabling the counter. When the counter is not armed, the bit is ignored.
1–0	G*i* Save	G*i* Save indicates the state of the SW Save register. It sets when the SW Save Register is latched for reading.

G01 Joint Status 1 Register

Address Offset: 0x036

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	Serial In Progress	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	G1 Gate	G0 Gate	G1 Bank	G0 Bank

Bits	Name	Description
12	Serial in Progress	This bit indicates that hardware serial-to-parallel conversion is in progress.
3–2	G*i* Gate	This bit reads the state of the selected gate signal after polarity selection.
1–0	G*i* Bank	This bit indicates which bank of A and B registers the counter is using. 0—Bank X 1—Bank Y

G23 Joint Status 1 Register

Address Offset: 0x136

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	G3 Gate	G2 Gate	G3 Bank	G2 Bank

Bits	Name	Description
3–2	G*i* Gate	This bit reads the state of the selected gate signal after polarity selection.
1–0	G*i* Bank	This bit indicates which bank of A and B registers the counter is using. 0—Bank X 1—Bank Y

G01 Joint Status 2 Register
G23 Joint Status 2 Register

Address Offsets: 0x03A (G01), 0x13A (G23)

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
G1 Permanent Stale Data	G0 Permanent Stale Data	G1 HW Save	G0 HW Save	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	G1 Output	G0 Output

Bits	Name	Description
15–14	G*i* Permanent Stale Data	This bit is set if the G*i* Stale Data bit is set at any time during counter operation. A counter reset clears this bit.
13–12	G*i* HW Save	Hardware Save. This bit indicates that it latched valid data and is ready to read.
1–0	G*i* Output	This bit allows the counter output state to be read back. The read occurs after the polarity selection.

G*i* SW Save Register

Address Offsets: 0x018 (G0), 0x01C (G1), 0x118 (G2), 0x11C (G3)

Type: Read

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
SW Save.31	SW Save.30	SW Save.29	SW Save.28	SW Save.27	SW Save.26	SW Save.25	SW Save.24

23	22	21	20	19	18	17	16
SW Save.23	SW Save.22	SW Save.21	SW Save.20	SW Save.19	SW Save.18	SW Save.17	SW Save.16

15	14	13	12	11	10	9	8
SW Save.15	SW Save.14	SW Save.13	SW Save.12	SW Save.11	SW Save.10	SW Save.9	SW Save.8

7	6	5	4	3	2	1	0
SW Save.7	SW Save.6	SW Save.5	SW Save.4	SW Save.3	SW Save.2	SW Save.1	SW Save.0

Bits	Name	Description
31–0	SW Save.<31..0>	Software Save. This value is latched on the next source edge following the assertion of the Save Trace bit. When the bit is clear, the counter value is transparent through the SW Save register. This register is also part of the buffer for DMA operations. When G*i* DMA Enable in the G*i* DMA Config register is set, the SW Save register is used as a HW Save register. In DMA mode, the save value alternates between the HW Save register and the SW Save register.

Simple Digital Input/Output

An 8-bit DIO port is available for simple unstrobed read and write operations.

STC Digital Input/Output

The 8-bit digital port provides individual control over the direction and state of each bit. This port is located on pins 0 through 7.

STC Digital Input/Output Registers

Table 3-2 shows the STC digital input/output register map. The table provides the register name, the register address offset from the device base address (Base Address Register 1), the type of register—read-only and write-only, and the size of the register in bits.

Registers are grouped in the table by offset.

Table 3-2. STC Digital Input/Output Register Address Map

Register Name	Offset (Hex)	Type	Size
STC DIO Parallel Input	0x00E	Read-only	16-bit
STC DIO Output	0x014	Write-only	16-bit
STC DIO Control	0x016	Write-only	16-bit
STC DIO Serial Input	0x038	Read-only	16-bit

STC DIO Parallel Input

Address Offset: 0x00E

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
DIN.7	DIN.6	DIN.5	DIN.4	DIN.3	DIN.2	DIN.1	DIN.0

Bits	Name	Description
7–0	DIN.<7..0>	Digital Input. This field reads the state of the STC DIO pins.

STC DIO Output

Address Offset: 0x014

Type: Write

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
Serial DOUT.7	Serial DOUT.6	Serial DOUT.5	Serial DOUT.4	Serial DOUT.3	Serial DOUT.2	Serial DOUT.1	Serial DOUT.0

7	6	5	4	3	2	1	0
Parallel DOUT.7	Parallel DOUT.6	Parallel DOUT.5	Parallel DOUT.4	Parallel DOUT.3	Parallel DOUT.2	Parallel DOUT.1	Parallel DOUT.0

Bits	Name	Description
15–8	Serial DOUT.<7..0>	Serial Digital Input. This field loads the output register to be shifted on the next serial start.
7–0	Parallel DOUT.<7..0>	Parallel Digital Output. This field immediately updates the STC DOUT pins when they are enabled for output drive.

STC DIO Control

Address Offset: 0x016
Type: Write
Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
0	0	0	0	Serial SW Strobe	Serial Timebase	Serial HW Enable	Serial Start

7	6	5	4	3	2	1	0
OE 7	OE 6	OE 5	OE 4	OE 3	OE 2	OE 1	OE 0

Bits	Name	Description
11	Serial SW Strobe	Serial Software Strobe. When HW Serial is disabled, Serial SW Strobe can toggle the serial clock.
10	Serial Timebase	0—Serial clock is Timebase 1 / 24 (1.2 µs) 1—Serial clock is Timebase 2 (100 KHz)
9	Serial HW Enable	Serial Hardware Enable. Setting this bit enables hardware parallel-to-serial conversion. Setting this bit causes serial clock to be driven on STC DOUT 4 and serial data out to be driven on STC DOUT 0.
8	Serial Start	Setting Serial Start initiates parallel-to-serial conversion of the Serial DOUT register, starting with bit 0. It also captures serial input into the serial input register. This bit automatically clears when the conversion completes. The Serial I/O Progress bit can monitor the conversion progress.
7–0	OE.<7..0>	Output Enable. These bits control the output enable for the STC DIO lines when using I/O pins 7 through 0 if these pins are programmed as inputs in the I/O configuration registers. This setting makes the port compatible with the DAQ STC. The I/O configuration registers also control the output enables, in which case these bits are ignored.

STC DIO Serial Input

Address Offset: 0x038

Type: Read

Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
Serial DIN.7	Serial DIN.6	Serial DIN.5	Serial DIN.4	Serial DIN.3	Serial DIN.2	Serial DIN.1	Serial DIN.0

Bits	Name	Description
7–0	Serial DIN.<7..0>	Serial Digital Input. These bits store the serial input data after hardware serial-to-parallel conversion completes.

I/O Connection Registers

The NI-TIO has a 40-pin I/O connector interface. These 40 bidirectional signals control most of the NI-TIO operations. The direction and output signals are programmable.

Note When the NI-TIO powers up, all I/O pins are in the common input usage state.

Pin Usage

Table 3-3 lists output sources and common inputs for each I/O connection pin.

Table 3-3. I/O Connection Pin Usage

Pin Number	Common Input Usage	Counter Output
PFI 0	STC DIN 0	STC DOUT 0
PFI 1	STC DIN 1	STC DOUT 1
PFI 2	STC DIN 2	STC DOUT 2
PFI 3	STC DIN 3	STC DOUT 3
PFI 4	STC DIN 4	STC DOUT 4
PFI 5	STC DIN 5	STC DOUT 5
PFI 6	STC DIN 6	STC DOUT 6
PFI 7	STC DIN 7	STC DOUT 7
PFI 8	—	Cntr 7 Output
PFI 9	Up/Down 7	—
PFI 10	Gate 7	Cntr 7 Selected Gate
PFI 11	Source 7	Cntr 7 Selected Src
PFI 12	—	Cntr 6 Output
PFI 13	Up/Down 6	—
PFI 14	Gate 6	Cntr 6 Selected Gate
PFI 15	Source 6	Cntr 6 Selected Src
PFI 16	—	Cntr 5 Output

Table 3-3. I/O Connection Pin Usage

Pin Number	Common Input Usage	Counter Output
PFI 17	Up/Down 5	—
PFI 18	Gate 5	Cntr 5 Selected Gate
PFI 19	Source 5	Cntr 5 Selected Src
PFI 20	—	Cntr 4 Output
PFI 21	Up/Down 4	—
PFI 22	Gate 4	Cntr 4 Selected Gate
PFI 23	Source 4	Cntr 4 Selected Src
PFI 24	—	Cntr 3 Output
PFI 25	Up/Down 3	—
PFI 26	Gate 3	Cntr 3 Selected Gate
PFI 27	Source 3	Cntr 3 Selected Gate
PFI 28	—	Cntr 2 Output
PFI 29	Up/Down 2	—
PFI 30	Gate 2	Cntr 2 Selected Gate
PFI 31	Source 2	Cntr 2 Selected Src
PFI 32	—	Cntr 1 Output
PFI 33	Up/Down 1	—
PFI 34	Gate 1	Cntr 1 Selected Gate
PFI 35	Source 1	Cntr 1 Selected Src
PFI 36	—	Cntr 0 Output
PFI 37	Up/Down 0	—
PFI 38	Gate 0	Cntr 0 Selected Gate
PFI 39	Source 0	Cntr 0 Selected Src

Registers

Register Name	Offset (Hex)	Type	Size
I/O Config Reg 0–3	0x77C	Read and Write	32-bit
I/O Config Reg 4–7	0x780	Read and Write	32-bit
I/O Config Reg 8–11	0x784	Read and Write	32-bit
I/O Config Reg 12–15	0x788	Read and Write	32-bit
I/O Config Reg 16–19	0x78C	Read and Write	32-bit
I/O Config Reg 20–23	0x790	Read and Write	32-bit
I/O Config Reg 24–27	0x794	Read and Write	32-bit
I/O Config Reg 28–31	0x798	Read and Write	32-bit
I/O Config Reg 32–35	0x79C	Read and Write	32-bit
I/O Config Reg 36–39	0x7A0	Read and Write	32-bit

I/O Config Register, Pins A through D

Address Offset: 0x77C, 0x780, 0x784, 0x788, 0x78C, 0x790, 0x794, 0x79C, 0x7A0

Type: Read and Write

Size: 32-bit

Bit Map:

31	30	29	28	27	26	25	24
X	A Input Select 2	A Input Select 1	A Input Select 0	X	X	A Output Select 1	A Output Select 0

23	22	21	20	19	18	17	16
X	B Input Select 2	B Input Select 1	B Input Select 0	X	X	B Output Select 1	B Output Select 0

15	14	13	12	11	10	9	8
X	C Input Select 2	C Input Select 1	C Input Select 0	X	X	C Output Select 1	C Output Select 0

7	6	5	4	3	2	1	0
X	D Input Select 2	D Input Select 1	D Input Select 0	X	X	D Output Select 1	D Output Select 0

Bits	Name	Description
25–24, 17–16, 9–8, 1–0	Output Select <1..0>	This field determines if the I/O pin is driven and what signal is driven into the pin. 00—Pin is input only; driver tristates 01—Normal counter output
30–28, 22–20, 14–12, 6–4	Input Select <2..0>	This field allows each input pin to be passed through or digitally filtered to remove noise. The digital filters sample the signal using Timebase 3, and upon detecting

a state change, require it to be in the same state for a minimum pulse width either internally generated or selected from a RTSI line.

000—Input signal unchanged
001—Input synchronized to Timebase 3
010—Digital filter; minimum pulse width is 100 assertions of Timebase 1
011—Digital filter; minimum pulse width is 20 assertions of Timebase 1
100—Digital filter; minimum pulse width is 10 assertions of Timebase 1
101—Digital filter; minimum pulse width is 2 assertions of Timebase 1
110—Digital filter; minimum pulse width is 2 assertions of Timebase 3

MITE

The MITE is located on PCI BAR0, offset 0x0.

To enable the BAR1 address space where the NI-TIOs are located, write to the I/O Device Window Base Size Register (IODWBSR) on the MITE. The IODWBSR determines the location of the I/O device window in the CPU address space. This window is used to access the DEVICE* address space on the I/O port.

For example, if the PCI/PXI device base address range 0 is BAR0, and the card base address range 1 is BAR1, enable BAR1 with the following:

```
Write32(BAR0 + 0xC0, (BAR1 & 0xFFFFFF00L) | 0x80)
```

I/O Device Window Base Size Register (IODWBSR)

Address Offset: 0xC0

Type: Read and Write

Size: 32-bit

Bit Map

31	30	29	28	27	26	25	24
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24

23	22	21	20	19	18	17	16
BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16

15	14	13	12	11	10	9	8
BA15	BA14	BA13	BA12	X	X	X	X

7	6	5	4	3	2	1	0
WENAB	X	X	X	X	X	X	WSIZE

Bits	Name	Description
31–12	BA <31..12>	Base Address. These bits indicate base address of the 8 KB device window in CPU address space, and are only valid when WENAB=1 and WSIZE=0.
7	WENAB	Window Enable. Setting this bit enables the window. Clearing this bit disables the window.
11–8, 6–1	X	X should always be written with a 0, and ignored when read.
0	WSIZE	Window Size. If WSIZE is set, the window size is 4 GB. If WSIZE is clear, the device region is 8 KB.

A

Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
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If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meaning	Value
μ-	micro-	10^{-6}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Symbols

°	degree
–	negative of, or minus
/	per
%	percent
±	plus or minus
+	positive of, or plus

A

A	amperes
ANSI	American National Standards Institute
API	application programming interface
arm	to enable a counter to start an operation. If the application requires a trigger, an armed counter waits for the trigger to begin the operation.
ASIC	application specific integrated circuit
asynchronous	a property of an event that occurs at an arbitrary time, without synchronization to a reference clock

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
base address	a memory address that serves as the starting address for programmable registers. All other addresses are located by adding to the base address.
buffer	a block of memory used to store measurement results
buffered	a type of measurement in which multiple measurements are made consecutively and measurement results are stored in a buffer
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the AT, EISA, and PCI bus.

C

C	Celsius
clock	hardware component that provides timing for various device operations
cm	centimeters
CMOS	complementary metal-oxide semiconductor
CompactPCI	an electrical superset of the PCI bus architecture with a mechanical form factor suited for industrial applications
crosstalk	an unwanted signal on one channel due to activity on a different channel
current drive capability	the amount of current a digital or analog output channel is capable of sourcing or sinking while still operating within voltage range specifications
current sinking	the ability of a DAQ board to dissipate current for analog or digital output signals
current sourcing	the ability of a DAQ board to supply current for analog or digital output signals

D

DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer
DAQ-STC	a custom ASIC developed by National Instruments that provides timing information and general-purpose counter/timers on National Instruments E Series boards
DC	direct current
decode	used in the context of motion encoders. The two channels of a motion encoder indicate information about movement and direction of movement of an external device. Decoding refers to extracting this information from the signals on these channels.
device	a plug-in data acquisition board, card, or pad that can contain multiple channels and conversion devices. Plug-in boards, PCMCIA cards, and DAQ devices that connect to your computer parallel port, are all examples of DAQ devices.
DIO	digital input/output
DLL	dynamic link library—a software module in Microsoft Windows containing executable code and data that can be called or used by Windows applications or other DLLs. Functions and data in a DLL are loaded and linked at run time when they are referenced by a Windows application or other DLLs.
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
driver	software that controls a specific hardware device such as a DAQ board
duty cycle	the percentage of the cycle in which the pulse is high.

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EISA	extended industry standard architecture
encode	used in the context of motion encoders. Motion encoders provide information about movement and direction of movement of an external device. The process of producing the pulses that contain this information is called encoding.
ETS	equivalent time sampling

F

FSK	frequency shift keying

G

GATE	the signal that controls the operation of a counter. This signal may start or stop the operation of a counter, reload the counter, or save the results of a counter.
glitch	a brief, unwanted change, or disturbance, in a signal level
GND	ground

H

hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, cables, and so on
HW	hardware
HW Save Register	a register inside the NI-TIO ASIC that stores the result of a measurement
Hz	hertz—a unit of frequency. One hertz corresponds to one cycle or event per second

I

in.	inches
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
IRQ	interrupt request signal
ISA	industry standard architecture

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench, a National Instruments graphical programming application

M

m	meters
max	maximum
maximum timebase	the fastest internal timebase available on a device. For 6601 devices, the maximum timebase is 20 MHz. For 6602 devices, the maximum timebase is 80 MHz.
min	minimum
MITE	a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high speed data transfers over the PCI bus.

motion encoders	transducers that generate pulses to indicate the physical motion of a device. The most common type of motion encoders are quadrature encoders. Two-pulse encoders (also referred to as up/down encoders) are another example.

N

NI-DAQ	NI driver software for DAQ hardware
NI-TIO	a custom ASIC developed by National Instruments that provides counter and digital I/O functionality
noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

O

operating system	base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	programmable function input
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of lines of digital input and/or output
ppm	parts per million
prescaling	the division of frequency of an input signal that is to be used as SOURCE of a counter

programmed I/O	a data transfer method in which the CPU reads or writes data as prompted by software
PXI	modular instrumentation standard based on CompactPCI developed by National Instruments with enhancements for instrumentation

Q

quadrature encoders	a motion encoder that has two channels: channels A and B. Pulses and phases of pulses on channels A and B carry information about degree and direction of movement. A third channel—channel Z—may also exist that provides a reference point for position.

R

reflection	a high-speed signal transition behaves like a wave and is reflected like a wave at an inadequately terminated endpoint. This phenomenon is referred to as reflection.
RG	reserved ground. Pins that are marked RG on the I/O connector are no-connects if you use the SH6868-D1 shielded cable, while they are ground pins if you use the R6868 unshielded ribbon cable.
ribbon cable	a flat cable in which the conductors are side by side
ringing	the oscillation of a signal about a high-voltage or low-voltage state immediately following a transition to that state
RTSI Bus	real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions

S

s	seconds
(HW) Save register	a register inside the NI-TIO ASIC that stores the result of a measurement
source	in the counter context, source refers to the signal that causes the counter to increment or decrement. In the context of signals, source refers to the device that drives a signal.

SOURCE	the signal that causes the counter to increment or decrement
start trigger	a TTL level signal having two discrete levels—a high and a low level—that starts an operation
synchronous	a property of an event that is synchronized to a reference clock

T

TC	terminal count—a strobe that occurs when a counter reaches zero from either direction
termination	matching of impedances at the end of a signal path to minimize reflections.
timebase	another term used for the SOURCE of a counter. Usually indicates an internal SOURCE provided by or derived from an onboard oscillator.
trigger	any event that causes, starts, or stops some form of data capture
tri-state	a third output state, other than high or low, in which the output is undriven
TTL	transistor-transistor logic
two-pulse encoder	a motion encoder that has two channels: channels A and B. Pulses on channel A indicate movement in one direction while pulses on channel B indicate movement in the opposite direction. This type of encoder is also referred to as up down encoder.

U

unstrobed digital I/O	a type of digital input or output in which software reads or writes the digital line or port states directly, without using any handshaking or hardware-controlled timing functions. Also called *immediate*, *nonhandshaking*, or *unlatched* digital I/O.
UP_DOWN	the signal that determines whether a counter increments or decrements

V

V	volts
VDC	volts direct current
V_{in}	volts in
VI	Virtual Instrument. A LabVIEW program; so-called because it models the appearance and function of a physical instrument.

W

wire	data path between nodes